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Carrier Shifting Algorithms for the Mitigation of Circulating Current in Diode Clamped MLI fed Induction Motor Drive

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ABSTRACT

Reduction of circulating current is one of the major considerations in inverter fed electrical drives. Diode clamped MLI enables higher output current per phase, thereby rating of the drive gets increased effectively. Various methods of triggering in the inverter legs creates better voltage profile and leads to the enabling of circulating current in the drive system. The induced circulating current flows through the apparatus neutral (N) and supply ground (G) is caused by the existence of parasitic capacitance. This circulating current may cause potential danger especially when parasitic capacitance poses large. In the past, different modulation techniques and conversion topologies have been introduced to minimize the flow of circulating current. However, these techniques lead to complexity, high cost, low voltage profile and efficiency due to lower modulation parameters. This paper proposes PS, POD, PD carrier shifting PWM algorithms for diode clamped MLI to tumbling the circulating current within the each phase of inverter legs. The performances of proposed algorithm, in terms of circulating current, THD, losses and efficiencies are analyzed theoreticallyand are validated via simulation and experimental results.

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1. INTRODUCTION

Inverters are widely used in different industrial applications for conditioning the power in adjustable speed drives and renewable energy system because of it's ability to generate the desired output profile [1]-[2]. Multi-level topologies are employed mainly to minimize the harmonics in the inverter's output and to reach the required voltage rating of the power equipments. Multilevel inverters are becoming more popular because of it's power rating, reduced harmonics and EM. The multilevel inverter contains three topologies namely diode-clamped (DC-MLI), cascaded inverters (H-bridge-MLI), capacitor clamped inverters (FC-MLI) [3]-[4]. The inverters have various types of modulation strategies to control the performance. Space Vector Modulation (SVM) is one of the most popular PWM techniques. The carrier based PWM strategy can be segregated into two types they are single carrier and multi carrier PWM. The diode clamped multilevel inverters are having some good advance features like stair case waveform and minimized harmonics, and it is having a advantage of controlling the medium voltage drives [5].

In diode clamped inverters, modulation techniques phase disposition (PD), phase opposition disposition (POD), alternative phase opposition disposition (APOD), PS (phase shift) gives best results in terms of constant carrier frequency not synchronized with the stator terminal frequency [6]-[7]. For diode clamped inverters, phase opposition disposition (POD) depends modulation strategy is widely used but it

offer a high harmonic performance [8]. Out of the modulation strategies the space vector PWM gives greater fundamental output voltage and improved harmonic performance of inverter.

The analysis of circulating current is more important in the AC motor drives application. It produces between neutral point (N) of the motor and supply ground (G). The existence of shaft voltage, bearing damage, etc are some of the major effect of circulating current.The concurrent switching of the series connected switches creates high dv/dt across load terminals of inverter. The increase in circulating current affects motor insulation and also the cables. In drive applications it may causes the electromagnetic interference (EMI) this noise causes to trip the inverter drive [9]. It is very essential to limit the circulating current to certain boundary. A MLI can reduce the circulating current. Output voltage of multilevel inverter will vary in small increments because of the more number of switching states [10], it allows to mitigate the low frequency harmonics thereby the switching loss will be reduced. Furthermore the circulating current can be reduced by reducing the dv/dt rate [11]. The cascaded inverter is widely implemented for the industrial applications in the literature [12]-[13], however the main drawback of this type of configuration is it requires isolation transformers on AC side and a more number of DC sources. Among all the configurations present in multilevel inverter, the analysis of circulating current is derived for the DC-MLI, which is the more frequent topology of the 3-level inverters. For medium and high voltage AC drives, this topology can be connected directly to power system utility.

The effect of shaft voltage and it's resulting current were studied by Alger in 1920's [14]. Various mechanical modifications in the system had been presented in the literature to eliminate the negative effects of the circulating current over motor bearing, like cable type, passive filters and the type of the bearing. There are two types of cables are available they are shielded type and unshielded type, the unshielded type of cable has no impact on the circulating currents. Even shielded type of cables also has no impact on small rating motors, in higher rated motors, the magnitude of circulating current is inversely proportional to the motor speed. P. pairodamonchai [15] has given the procedure for designing and complications while designing passive filters. There are 4 types of filters are available to eliminate the circulating current they are dv/dt filters (11 kW power level) and dv/dt reactors (110 and 500 kW power levels), sinusoidal filters [16], and common-mode chokes [17]. The elimination of bearing current is 30 to 90% [18]-[19] based on the type of the filter on large rating motors and there is no impact [20] in small rating motors. Moreover the passive filters have more size and weight penalties. There are two types of bearings are available insulated bearing [21]-[22] and hybrid bearing. Insulated bearing eliminates 40 to 60% of the circulating current on small rating motors and 60 to 80% [23] on large rating motors. Hybrid bearings give complete suppression of bearing currents in small motors not suitable for the large motor applications [24].

Different PWM technique provides different values of circulating current in the inverter. In this paper the circulating current suppression is proposed with the different modulation strategies. A three level DC-MLI is designed to drive 400 V, three-phase induction motor. Sinusoidal PWM, PD-SPWM, POD-SPWM, PS-SPWM techniques are implemented using a Matlab-2013b for the modulating index, ma=0.9 and switching frequency of 1050 Hz. The partial elimination of circulating current implemented using FPGA-SPARTEN III processor. The Simulation output and experimental results are provided to validate the circulating current in three-level diode clamped inverter [DC-MLI].

2. EFFECT OF HIGH CIRCULATING CURRENTS

The circulating current can be defined as the current that exists between the application neutral and ground.

$$I_{NG} = \frac{I_{AN}+I_{BN}+I_{CN}}{3} \quad (1)$$

The shaft voltage on the rotor side of the motor is induced due to common mode voltage with higher voltage and frequency in modern PWM inverter. If the breakdown voltage of lubricant in the bearing of motor is lesser then the induced shaft voltage, circulating current in larger value will be flow through the apparatus neutral (N) and supply ground (G) [21].

$$i_c = C_b \frac{dV_b}{dt} \quad (2)$$

$$i_c = BVR.\, C_b \frac{dV_{NG}}{dt} \quad (3)$$

Where BVR is the bearing voltage ratio.

This circulating current cause the malfunctioning of the sensitive electronic equipment such as in control systems, false tripping of the ground fault relays. In rotating electrical machines, this current damages the bearing which in turn damages the machine and also cause electromagnetic Interference. The instantaneous current sum is called as the circulating current. The generation of circulating current can be observed from the following Figure 2.

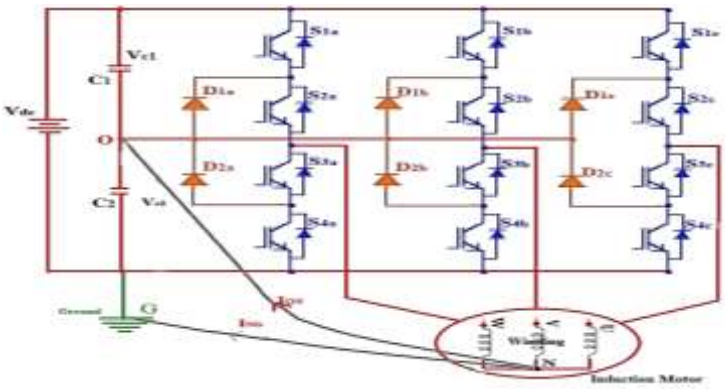

Figure 2. Circuit diagram of three-level NPC induction motor drive with circulating current

3. CARRIER SHIFTING ALGORITHMS

To generate the required PWM signal in the carrier based pulse width modulation, triangular carrier wave is compared with the reference sine wave.

3.1. Single Carrier PWM

The SPWM is a one of the most popular modulation techniques in the voltage source inverter. In Sinusoidal pulse width modulation, single triangular carrier wave is compared with the reference sine wave in order to generate firing signals for switching of the power electronic devices. In the medium voltage applications power dissipation is one of the most common problems. The open loop SPWM control method at fundamental frequency is to minimize the switching losses.

3.2. Multi Carrier PWM

The multi carrier PWM technique is employed only for the multi-level inverter. This technique is used to increase the efficiency of the inverter output. In this PWM technique the carrier waves are in two ways, they are horizontal and vertical. The vertical carrier distribution techniques are classified into two configurations they are Phase Disposition (PD), Phase opposition Disposition (POD), where horizontal distribution arrangement is only one type and that is Phase Shift (PS) control technique.

3.2.1. Phase disposition (PD)

The phase disposition is one of the techniques in the multi carrier PWM. In this type of technique, the number of carriers depends upon the number of levels in the inverter. The formula for knowing the number of carriers is (m-1), where m is number of levels. All carriers should be in phase disposition (PD, the PD-PWM is best suited for the NPC). We can observe this technique from the Figure 3(a).

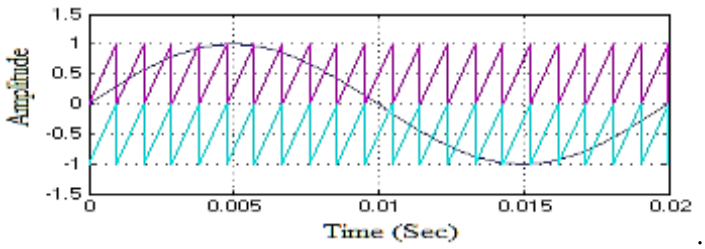

Figure 3(a). Phase Disposition

3.2.2. Phase opposition disposition (POD)

The number of carriers is (m-1), and all these carriers are in phase with zero reference. The carriers those are above the zero reference are in phase, but the carriers below zero reference are in phase opposition. The Figure 3(b) represents the POD technique.

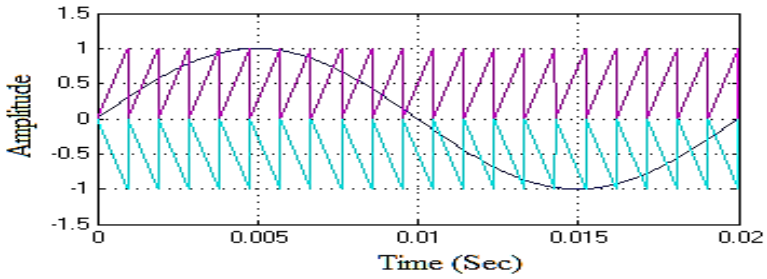

Figure 3(b). Phase Opposition Disposition

3.2.3. Phase shift (PS)

The number of carriers is (m-1), and each carrier is shifted by an angle of 90 degree accordingly. The Figure 3.2.3 represents the phase shift technique.

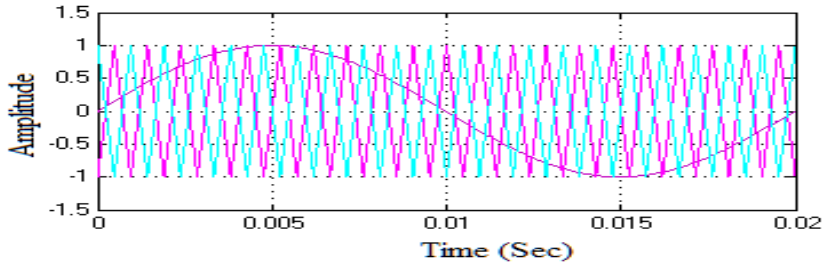

Figure 39(c). Phase Shift

4. ANALYSIS OF CIRCULATING CURRENT DEPENDS ON SWITCHING STATES

The circulating currents have been discussed for the different switching states available in the sections. The circulating current can be stated as the current between the application neutral and the ground point of the inverter. Magnitude of circulating current depends on the amount of the inverter input current. In the balanced star connected load the sum of phase currents are zero.

The three-level NPC inverter produces different combinations of the phase current depends on the switching states. There are 27 possible different switching states are available, each switching state has different amount of circulating current. The state 1 produces the phase current of $+I_{dc}/2$, 0 state produces 0A& -1 state produces $-I_{dc}/2$. All over 12 switching states produces $\pm I_{dc}/6$, 7 states produces zero circulating current, 6 states produce $\pm I_{dc}/3$& 2 states produce $\pm I_{dc}/2$. Some sample different switching states and their circulating current shown in the Figure 4.

5. CIRCULATING CURRENT REDUCTION

The circulating current minimization can be done by avoiding the abnormal switching of inverter. The PWM techniques like PD, POD, and PS can control the circulating current to such an extent, though the controlling of switching operation is not possible. The above chapter gives the detailed analysis of the available switching states and corresponding circulating current. From that analysis selecting the proper switching states the circulating current can be minimized. In the partial reduction of circulating current can be eliminated up to $I_{dc}/3(n-1)$ for n-level inverter. In the partial elimination the 3-level inverter allows the circulating current magnitude of $\pm I_{dc}/6$. Harmonics is inversely proportional to the common mode voltage. This shows that the reduction of harmonics can be achieved by eliminating the common mode voltage.

Similarly the circulating current is directly proportional to the harmonics. The amount of harmonics will decrease with the reduction of the circulating current. Different PWM techniques like PS, PD, POD will reduce the circulating current to such an extent. The PS PWM technique eliminates only till the level of $\pm I_{dc}/2$. The PD technique will reduce the circulating current till $\pm I_{dc}/6$.

The necessity to reduce the circulating current is more in order to protect the device from the failures. Finally the POD algorithm will reduce the circulating current till $\pm I_{dc}/3$. By comparing all the above results the best algorithm to reduce the circulating current is PD algorithm type. As we know already the circulating current directly proportional to the harmonics. So the harmonic level in the PD technique is comparatively low compared to all different algorithms.

6. SIMULATION RESULTS

The circulating current reduction for PD, POD, PS for 3-phase 3-level NPC-NLI has been simulated using matlab simulink to supply the drive system with 2.2Kw, 1440 RPM induction motor. The machine parameters are rated voltage =380V, rated current=5A, stator resistance=2.9Ω, rotor resistance=2.2Ω, stator leakage induction=12mH, rotor leakage induction=12mH& mutual induction=290mH. An open loop v/f speed control method is used to control the speed of the motor and DC-link set at 440V. Both the simulation and experimental results are carried out for 1 KHz switching frequency and modulation index of 0.877 at 50 Hz. The matlab simulation and experimental results for the partial elimination of circulating current at neutral is shown in the Figure 6. In the following figures, the observation that can be made is what is the amount of current is present and what is the amount of the circulating current eliminated. When compared to the three different PWM techniques the PD technique provides good results in terms of the circulating current and in terms of the harmonics. Ths is the partial elimination technique of the circulating current, with this complete elimination is not possible in order to eliminate completely this technique is not valid. The simulation which are provided in the Figure 6 are closely matching with the experimental results which are provided in Figure 7.

7. EXPERIMENTAL RESULTS

In this section, theoretical and simulation results for a 1 KW load system are shown. All waveforms shown in this section are captured from FPGA SPARTAN-III-3AN-XC3S400. The simulated MATLAB code connected with FPGA board through System generated tool, which ensure the less computational complexity environment [25]. Three phase three level IGBT based NPC inverter system was used to experimentally investigate the performance of the proposed topology. Figure 7(a) shows the output voltage (b) shows the pulse generation for the PD technique Figure 7(c) shows the circulating current. The following waveforms represent the voltage output, pulse generation and circulating current respectively. The IGBT used here is IRG4BC20FD with a fundamental frequency of 50 Hz and switching frequency of 1 kHz. The input DC bus voltage is 150V. 1 KW motor with 50 mH inductance and 15nF capacitance is used here. The circulating current mitigated using the PD technique is ±Idc/6 and that can be observed from the following diagram and the performance of the system is improved in terms of harmonics.

8. CONCLUSION

Premature failure of the bearings in the conventional two-level inverter is due to the induced circulating current in it. Multi-level inverters have their intrinsic ability to lessen the circulating current. Simulation and experimental results prove that the magnitude of the circulating current minimized to ±Idc/6, and that has a minimum THD in the line voltage and currrent. A multi-level inverter eliminates the dv/dt in its output voltage and therefore the circulating current will also gets reduced. In the conventional two level inverter this operation is not possible and that cause the premature failure of the bearings. The proposed three different PWM techniques will also decrease the cost of reduction. Thus when compared to the two level inverter the multi-level inverters has lot of advantages in terms of leakage current and harmonics.

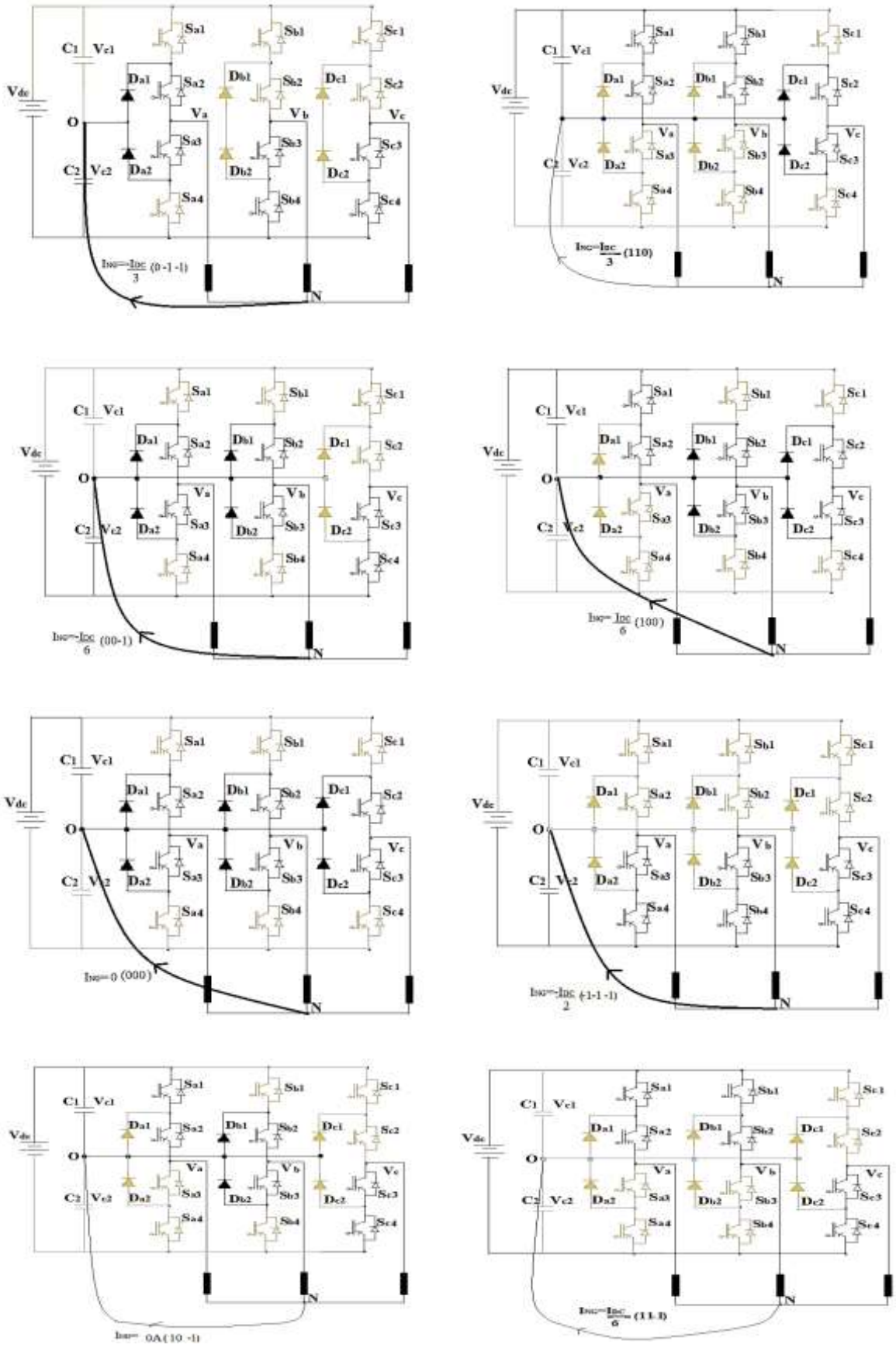

Figure 4. Different Switching states and its Circulating Current

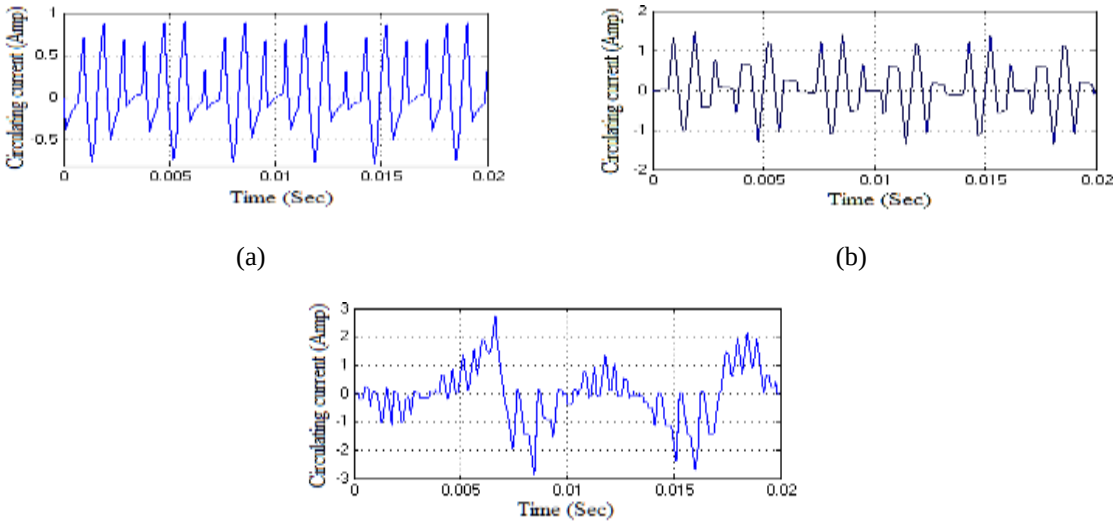

Figure 6. Simulation results (a) 3-level DC-MLI using PD ($I_{dc}/6$) , (b) 3-level DC-MLI using POD ($I_{dc}/3$), (c) 3-level DC-MLI using PS ($I_{dc}/2$)

Table 1. Result Comparision

PWM technique	THD	Circulating current
PD	51.36	$+I_{dc}/6$
POD	59.82	$+I_{dc}/3$
PS	89.48	$+I_{dc}/2$

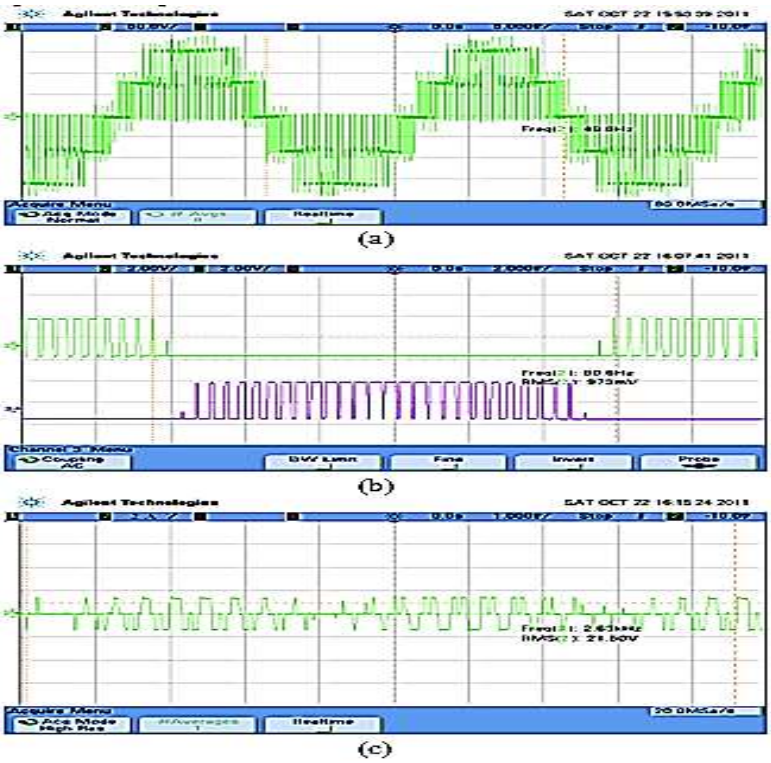

Figure 7. Experimental results for PD technique (a) Output voltage (50V/div) (b) pulse generation (2A/div) (c) circulating current (2A/div)

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